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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/671,888	09/29/2003	Fred Gehrung Gustavson	YOR920030169US1 YOR.463	7987

21254 7590 11/28/2007

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EXAMINER	
NGO, CHUONG D	
ART UNIT	**PAPER NUMBER**
2193	

MAIL DATE	DELIVERY MODE
11/28/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/671,888	GUSTAVSON ET AL.	
	Examiner	Art Unit	
	Chuong D. Ngo	2193	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 September 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4-9,17-19 and 21-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4-9,17-19 and 21-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *2 pages*.
4) ☒ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. The amendment filed on 06/19/2007 has been entered. Claims 1,2,4-9,17-19 and 21-29 are pending for further examination.

2. Claims 2,5-9,17-19 and 21-29 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As per claim 21, "said data registers of said co- processing unit", lines 3-4 lacks a proper antecedent basis. This problem is also found in claim 27. Further, it is unclear what it by the recitation "said position ... comprises loading said matrix data onto a set of said data registers of said cop processing unit", lines 2-4. (note: a position is incapable of performing a function)

As per claim 2, the limitation of the recitation "using a deviation from a normal floating point loading instruction", lines 5-6, is indefinite because "a normal floating point loading instruction" itself is unclear as to what is considered "a normal floating point loading instruction". Thus, what is considered "a deviation from a normal floating point loading instruction" is also unclear. Further, since known floating point loading instructions are not unique, any floating point loading instruction can be seen as a normal or a deviation from another normal floating point loading instruction. Therefore, the limitation of the recitation "using a deviation from a normal floating point loading instruction" is unclear.

As per claim 17, it is unclear what it means by the recitation "said register data block format converting the matrix ...", line 16, (note a format is incapable of performing a function).

As per claim 23, the recitation "each optimal matrix format", line 10, is indefinite and lacks a proper antecedent basis, since only "an optimal matrix format" recited on lines 8-9.

As per claim 24, "said pseudo matrix", line 2, and "each said pseudo matrix" lack proper antecedent basis.

As per claim 26, "said disadvantage", line 8, lacks a proper antecedent basis.

As per claim 28, the recitation "a method of overcoming a hardware disadvantage on said computer relative to a specific processing on a specific computer architecture/set of instructions", lines 6-8, is indefinite as to what is the "hardware disadvantage", what is the "specific processing" and what are the "specific computer architecture/set of instructions". Further, the limitations of the recitations "a first error relative to said specific processing", line 11, and "a correcting error relative to said specific processing", line 12, are also indefinite as to what can be seen as "a first error relative to said specific processing", and "a correcting error relative to said specific processing". The scope of the recitations on lines 6-15 is indefinite, since any computer device can be seen as to have a hardware disadvantage, and a part of a process performed in the computer can seen as to generating an error, and another part of the process can be seen as to correct the error to overcome the disadvantage. The claim should recite what the first software instructions do in process input data to generate a first error, and what the second software instructions do in process input data to correct the error in order to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

3. Claims 17-19 are rejected under 35 U.S.C. 102(e) as being clearly anticipated by Lao et al. (7,031,994).

As per claims 17, Lao et al discloses matrix operation on matrix data stored in a standard format in the memory, including (step 1, see col. 9, lines 28-50) separating the matrix (A) into blocks, rearrange and placing in the memory said block by reading each block in row-wise to the workspace sequentially, then writing back in column-wise into their original spots in the memory. The separation of matrix and rearrangement of blocks (step 1) clearly result in a matrix (A1) having blocks of data to be contiguous blocks of contiguous data stored in the memory in a nonstandard format that permits said matrix data (A1) to be moved from said storage memory system into a position for performing said matrix operation (matrix transpose) more quickly than if said matrix data had been moved as stored in said standard format as claimed. Further, Lao similarly discloses in Col. 16 matrix operation including separating a matrix (A) into blocks of size 2-by-2 (Col. 16, lines 27-35); rearrange and storing the blocks of data (Col. 16, lines 35-45) into contiguous blocks of contiguous data (col.16, lines 43-35) in a nonstandard format as claimed.

As per claims 18 and 19, Lao also discloses in Col. 16, line 37-58, repetitively loading the blocks using 2x2 crisscrossing technique to form a transpose data (AT) of the matrix (A).

4. Claims 1,4,23,24,26,28 and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lao et al. (7,031,994) in view of Gulley et al (5,025,407).

As per claims 1,4,23,24,26,Lao et al discloses in figure 6 an apparatus having a processor (600), a memory system (602) and a plurality of data register (202,604), for perform matrix operation on matrix data stored in a standard format in the memory, including (step 1, see col. 9, lines 28-50) separating the matrix (A) into blocks, rearrange and placing in the memory said

block by reading each block in row-wise to the workspace sequentially, then writing back in column-wise into their original spots in the memory. The separation of matrix and rearrangement of blocks (step 1) clearly result in a matrix (A1, col. 9, lines 47-50) having blocks of data to be contiguous blocks of contiguous data in the memory such that said matrix data is represented in a nonstandard format that permits said matrix data (A1) to be moved from said storage memory system into a position for performing said matrix operation (matrix transpose) more quickly than if said matrix data had been moved as stored in said standard format as claimed. Further, Lao similarly discloses in Col. 16 matrix separation including separating a matrix (A) into blocks of size 2-by-2 (Col. 16, lines 27-35); rearrange and storing the blocks of data into contiguous blocks of contiguous data (col.16, lines 35-45) in a nonstandard format as claimed. It is noted that Lao et al. does not specifically disclose co-processor unit. However, Gulley et al. discloses in figure 2 floating point coprocessor (1200) having matrix capabilities in addition to a processor (200). It would have been obvious to a person of ordinary skill in the art to provide the apparatus of Lao et al. with a floating point coprocessor as taught by Gulley in order to increase the speed of processing.

As per claims 28 and 29 the instructions that cause the apparatus to perform step 1, in col. 9, lines 28-50 or in col. 16, lines 27-45, are seen as the claimed first software instructions to preliminarily process input data in a manner to generate a first error relative, and ,the instructions that cause the apparatus to perform step 2, in col. 9, line 51 to col. 10, lines 11, or in col. 16, lines 46-57, are seen as the claimed second software instructions to subsequently process said input data in a manner to generate a correcting error.

5. Applicant's arguments filed on 06/19/2007 and 09/18/2007 have been fully considered but they are not persuasive.

It is respectfully submitted the rearranged matrix A1 (col. 9, lines 47-50) and the rearranged matrix in Col. 16, lines 27-35 clearly have blocks of data to be contiguous blocks of contiguous data stored in the memory in a nonstandard format which is not a normal or transpose format of the original matrix A and thus is not in a column major format or a row major format as claimed.

6. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chuong D. Ngo whose telephone number is (571) 272-3731. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai An can be reached on (571) 272-3756. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Chuong D Ngo/
Primary Examiner
Art Unit 2193

11/21/2007